REMARKS

Claims 1-18 are pending in the present application. Claims 1-5 and 8-15 have been amended. Claims 17 and 18 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Drawings

Enclosed is one (1) red-inked drawing Annotated Sheet, wherein output 127 of Comparator 106 has been denoted as "noncoincidence signal", and the signal provided to input G of data latch 103 has been denoted as 121, to improve accuracy. Also enclosed is one (1) drawing Replacement Sheet, incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheet.**

Claim Rejections-35 U.S.C. 102

Claims 1-4, 6, 8-12, 14 and 15 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Tuda et al. reference (U.S. Patent No. 5,132,937). This rejection is respectfully traversed for the following reasons.

The circuit for detecting an abnormal operation of memory of claim 1 includes in

combination a delay circuit "for delaying an output data output from the memory for a predetermined period of time and for outputting a delay data responsive thereto"; and a comparison circuit "for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose these features.

Applicant respectfully notes that the reasons as provided by the Examiner with respect to this rejection are unclear. For example, at the top of page 3 of the current Office Action dated April 10, 2006, the Examiner has directed attention to Fig. 6, column 4, lines 2-41 of the Tuda et al. reference with respect to the delay circuit of claim 1. However, column 4, lines 2-41 of the Tuda et al. reference makes reference to Figs. 3A, 3C and 3D, not Fig. 6. Moreover, the Examiner has relied on Fig. 6, column 2, lines 44-60 of the Tuda et al. reference with respect to the comparison circuit of claim 1. However, column 2, lines 44-60 of the Tuda et al. reference does not specifically make reference to Fig. 6.

Particularly, the Examiner has not specifically identified the circuit elements in Fig. 3A and/or Fig. 3C of the Tuda et al. reference that have been respectively interpreted as the delay circuit and the comparison circuit of claim 1. For instance, both Figs. 3A and 3C of the Tuda et al. reference are referred to in the passage relied upon by the Examiner, and respective delay circuits 212 and 211a are shown in Figs. 3A and 3C. Since the Examiner has not specifically identified by reference numeral the circuit

elements of the Tuda et al. reference that have been interpreted as the delay circuit and the comparison circuit of claim 1, the record with respect to this rejection is unclear.

The Examiner has presumably interpreted address change detecting circuit 211 in Fig. 3A of the Tuda et al. reference as the comparison circuit of claim 1. However, as described beginning in column 4, line 2 of the Tuda et al. reference, address change detecting circuit 211 detects changes of the input column address signal Adc and the row address signal Adr. Address change detecting circuit 211 does not compare output data output from a memory and delayed data, as would be necessary to meet the features of claim 1. That is, address change detecting circuit 211 receives a column address signal Adc and a row address signal Adr, and outputs an ADT pulse responsive thereto. Address change detecting circuit 211 of the Tuda et al. reference does not output a noncoincidence signal, as would be necessary to meet the further features of claim 1. Address change detecting circuit 211 therefore cannot be interpreted as the comparison circuit of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 distinguishes over the Tuda et al. reference as apparently relied upon by the Examiner, and that this rejection of claims 1-4 and 6 is improper for at least these reasons.

With further regard to claim 1, the Examiner has apparently interpreted delay circuit 212 in Fig. 3A of the Tuda et al. reference as the delay circuit of claim 1. However, delay circuit 212 merely delays the ATD pulse output from address change detecting circuit 211. Delay circuit 212 of the Tuda et al. reference does not delay an

output data output from a memory, and does not provide delayed data responsive thereto, as would be necessary to meet the further features of claim 1. Delay circuit 212 in Fig. 3A of the Tuda et al. reference therefore cannot be interpreted as the delay circuit of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 distinguishes over the Tuda et al. reference as relied upon by the Examiner, and that this rejection of claims 1-4 and 6 is improper for at least these additional reasons.

Regarding claim 2, the Examiner has very generally asserted that column 4, lines 45 through to column 5, line 25 and Fig. 6 of the Tuda et al. reference **explicitly** teach an access speed of a memory as detected. However, the above noted portions of the Tuda et al. reference as relied upon do not specifically describe, mention, or consider access speed of a memory, or more particularly detection thereof. In contrast, a result storing mode is described in column 5 of the Tuda et al. reference. Applicant therefore respectfully submits that claim 2 distinguishes over the Tuda et al. reference as relied upon by the Examiner for at least these additional reasons.

Regarding claim 3, since the Tuda et al. reference as relied upon by the Examiner does not disclose a comparison circuit that outputs a noncoincidence signal when output data from a memory and delayed data are not coincident with each other, the Tuda et al. reference clearly does not explicitly or otherwise teach a circuit that holds address information in the case of noncoincidence in response to a noncoincidence signal, as asserted by the Examiner. Regarding claim 6, column 4,

lines 2-41 and column 5, lines 67 through to column 6, lines 3 of the Tuda et al. reference do not explicitly or otherwise teach that delay circuit 212 in Fig. 3A has a delay time that can be adjusted, as would be necessary to meet the features of claim 6. Applicant therefore respectfully submits that claims 3 and 6 respectively distinguish over the relied upon prior art for at least these additional reasons.

The integrated circuit of claim 8 includes in combination a memory; a delay circuit "which delays an output data from the memory and outputs a delayed data responsive thereto"; and a comparison circuit "which compares the output data from the memory and the delayed data, and which outputs a noncoincidence signal when the output data and the delayed data are not coincident".

Applicant respectfully submits that for at least somewhat similar reasons as set forth above with respect to claim 1, the Tuda et al. reference as relied upon by the Examiner does not disclose the features of claim 8. The delay circuit 212 in Fig. 3A of the Tuda et al. reference delays an ATD pulse output from address change detecting circuit 211, not data output from a memory, as would be necessary to meet the features of claim 8. Also, address change detecting circuit 211 has input thereto column address signal Adc and row address signal Adr, and therefore does not compare output data from a memory and delayed data to output a noncoincident signal, as would be necessary to meet the further features of claim 8. Applicant therefore respectfully submits that claim 8 distinguishes over the Tuda et al. reference as relied upon by the Examiner, and that this rejection is improper for at for at least these reasons.

Applicant also respectfully submits that the method for detecting an abnormal operation of memory of claim 9 distinguishes over the Tuda et al. reference for at least somewhat similar reasons as set forth above with respect to claim 1. Particularly, delay circuit 212 in Fig. 3A of the Tuda et al. reference does not delay an output data output from a memory. Also, address change detecting circuit 211 in Fig. 3A of the Tuda et al. reference does not output a noncoincidence signal when an output data output from a memory and delayed data are not coincident with each other. Applicant therefore respectfully submits that the method for detecting an abnormal operation of memory of claim 9 distinguishes over the Tuda et al. reference as relied upon by the Examiner, and that this rejection of claims 9-12,14 and 15 is improper for at for at least these reasons.

With further regard to this rejection, Applicant respectfully submits that the Tuda et al. reference as specifically relied upon does not detect access speed of the memory as featured in claim 10, and does not hold address information in case of noncoincidence in response to a noncoincidence signal as featured in claim 11. Moreover, since delay circuit 212 in Fig. 3A of the Tuda et al. reference is not described as having adjustable delay time, the Tuda et al. reference does not disclose the features of claim 15. Applicant therefore respectfully submits that claims 10,11 and 15 respectively distinguish over the Tuda et al. reference for at least these additional reasons.

Claim Rejections-35 U.S.C. 103

Claims 5, 7, 13 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tuda et al. reference. Applicant respectfully submits that the Tuda et al. reference as herein relied upon does not overcome the deficiencies as noted above with respect to the Tuda et al. reference. Applicant therefore respectfully submits that this rejection is improper for at least these reasons.

Claims 17 and 18

Applicant respectfully submits that claims 17 and 18 distinguish over the Tuda et al. reference, at least by virtue of dependency upon claim 8. With regard to claim 17, the Tuda et al. reference does not appear to include first and second latch circuits. With regard to claim 18, the Tuda et al. reference does not provide a noncoincidence signal as featured, and thus does not include an address information storing circuit which stores address information when a noncoincidence signal is output by a comparison circuit.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to August 10, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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Enclosures: One (1) drawing Annotated Sheet
One (1) drawing Replacement Sheet

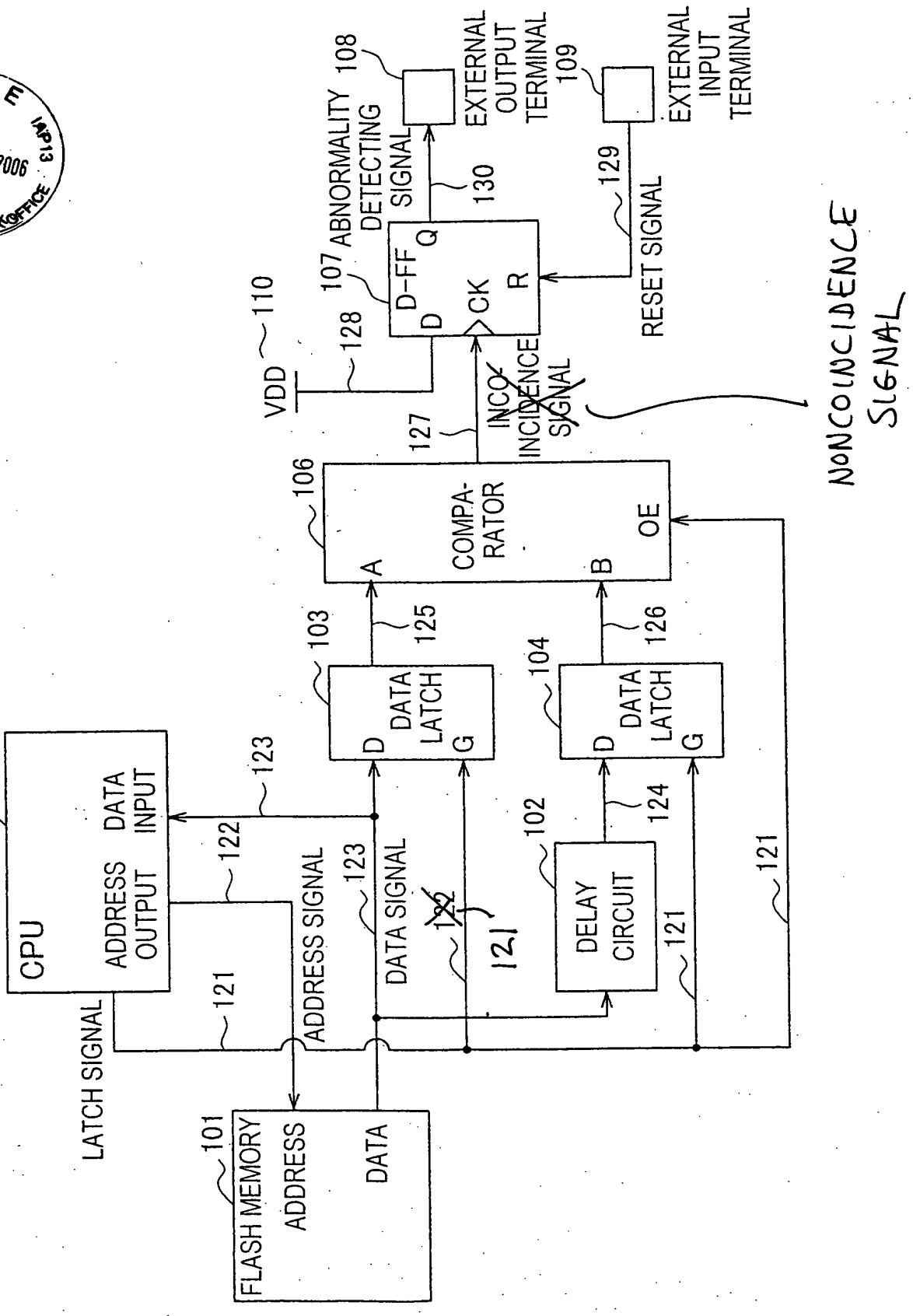

FIG.1